IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method for estimating jitter in a phase locked loop, comprising:

    obtaining a representative power supply waveform having noise;

    digitizing the representative power supply waveform having noise;

    ~~inputting the digitized representative power supply waveform having noise into a simulation of the phase locked loop~~

    simulating operation of the phase locked loop using the digitized representatively power supply waveform having noise as a power supply input to the phase locked loop; and

    estimating jitter of the phase locked loop ~~from the simulation~~based on the simulating.

2. (Original) The method of claim 1, wherein the representative power supply waveform is obtained from a physical system.

3. (Original) The method of claim 2, wherein the physical system comprises a printed circuit board.

4. (Original) The method of claim 2, wherein the physical system comprises a chip package.

5. (Original) The method of claim 2, wherein the physical system comprises a chip.

6. (Original) The method of claim 1, wherein the representative power supply waveform is obtained from a location on a physical system adjacent to an intended location of the phase locked loop.

7. (Original) The method of claim 1, wherein the representative power supply waveform is obtained from a simulation of a power supply.

8. (Previously Presented) A method for estimating jitter in a phase locked loop, comprising:

inputting a representative power supply waveform having noise into a simulation of the phase locked loop; and

estimating jitter of the phase locked loop from the simulation,

wherein the representative power supply waveform is obtained from a simulation of a power supply,

wherein the simulation of the power supply is performed using a first simulation tool and the simulation of the phase locked loop is performed using a second simulation tool.

9. (Original) The method of claim 1, wherein the representative power supply waveform comprises a noise waveform combined with a power supply waveform.

10. (Original) The method of claim 1, wherein the representative power supply waveform is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

11. (Original) The method of claim 1, wherein the simulation of the phase locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

12. (Currently Amended) A computer system for estimating jitter in a phase locked loop, comprising:

a processor;

a memory; and

software instructions stored in the memory adapted to cause the computer system to:

obtain a representative power supply waveform having noise;

digitize the representative power supply waveform having noise;

~~input the digitized representative power supply waveform having noise into a simulation of the phase locked loop~~

simulate operation of the phase locked loop using the digitized representatively power supply waveform having noise as a power supply input to the phase locked loop; and

estimate jitter of the phase locked loop from the simulation.

13. (Original) The computer system of claim 12, wherein the representative power supply waveform is obtained from a physical system.

14. (Original) The computer system of claim 13, wherein the physical system comprises a printed circuit board.

15. (Original) The computer system of claim 13, wherein the physical system comprises a chip package.

16. (Original) The computer system of claim 13, wherein the physical system comprises a chip.

17. (Original) The computer system of claim 12, wherein the representative power supply waveform is obtained from a location on a physical system adjacent to an intended location of the phase locked loop.

18. (Original) The computer system of claim 12, wherein the representative power supply waveform is obtained from a simulation of a power supply.

19. (Previously Presented) A computer system for estimating jitter in a phase locked loop, comprising:

a processor;

a memory; and

software instructions stored in the memory adapted to cause the computer system to:

input a representative power supply waveform having noise into a simulation of the phase locked loop; and

estimate jitter of the phase locked loop from the simulation;

wherein the representative power supply waveform is obtained from a simulation of a power supply, and

wherein the simulation of the power supply is performed using a first simulation tool and the simulation of the phase locked loop is performed using a second simulation tool.

20. (Original) The computer system of claim 12, wherein the representative power supply waveform comprises a noise waveform combined with a power supply waveform.

21. (Original) The computer system of claim 12, wherein the representative power supply waveform is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

22. (Original) The computer system of claim 12, wherein the simulation of the phase locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

23. (Currently Amended) A computer-readable medium having recorded thereon instructions executable by a processor, the instructions adapted to:

obtain a representative power supply waveform having noise;

digitize the representative power supply waveform having noise;

~~input the digitized representative power supply waveform having noise into a simulation of a phase locked loop~~

simulate operation of a phase locked loop using the digitized representatively power supply waveform having noise as a power supply input to the phase locked loop; and

estimate jitter of the phase locked loop from the simulation.

24. (Original) The computer-readable medium of claim 23, wherein the representative power supply waveform is obtained from a physical system.

25. (Original) The computer-readable medium of claim 24, wherein the physical system comprises a printed circuit board.

26. (Original) The computer-readable medium of claim 24, wherein the physical system comprises a chip package.

27. (Original) The computer-readable medium of claim 24, wherein the physical system comprises a chip.

28. (Original) The computer-readable medium of claim 23, wherein the representative power supply waveform is obtained from a location on a physical system adjacent to an intended location of the phase locked loop.

29. (Original) The computer-readable medium of claim 23, wherein the representative power supply waveform is obtained from a simulation of a power supply.

30. (Previously Presented) A computer-readable medium having recorded thereon instructions executable by a processor, the instructions adapted to:

input a representative power supply waveform having noise into a simulation of a phase locked loop; and

estimate jitter of the phase locked loop from the simulation,

wherein the representative power supply waveform is obtained from a simulation of a power supply, and

wherein the simulation of the power supply is performed using a first simulation tool and the simulation of the phase locked loop is performed using a second simulation tool.

31. (Original) The computer-readable medium of claim 23, wherein the representative power supply waveform comprises a noise waveform combined with a power supply waveform.

32. (Original) The computer-readable medium of claim 23, wherein the representative

power supply waveform is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

33. (Original) The computer-readable medium of claim 23, wherein the simulation of the phase locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.